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TITLE OF THE INVENTION (280 characters maximum)

**COMPLEX OXIDES FOR USE IN SEMICONDUCTOR DEVICES AND  
RELATED METHODS**

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- ☒ Drawing(s) (Number of Sheets 10)
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Carey Gregory

## COMPLEX OXIDES FOR USE IN SEMICONDUCTOR DEVICES AND RELATED METHODS

### Field of the Invention

[0001] The invention generally relates to oxides that may be used in conjunction with integrated circuit devices, e.g., field effect transistors and high electron mobility transistors, as well as other devices including photovoltaics, and methods of making the same.

### Background of the Invention

[0002] Insulated gate field effect transistors (IGFETs) typically include a channel region in which current is controlled through the application of an electrical bias to a gate electrode that is separated from the channel region by a thin insulating film or gate dielectric. Current through the channel is supplied and collected by source and drain contacts, respectively, to the channel region. As semiconductor devices become increasingly miniaturized, gate dielectrics having a reduced equivalent oxide thickness (EOT) may be desirable. For example, the Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) currently projects that gate dielectrics with an EOT below 1 nm may be desirable for uses such as in advanced complementary metal-semiconductor oxide field-effect transistor (CMOS FET) devices having channel lengths scaled to below 50 nm. However, reduced EOT dielectrics may exhibit tunneling and current leakage. For example, tunneling of conventional materials such as  $\text{SiO}_2$  may exceed  $1\text{-}5 \text{ } / \text{cm}^2$  at applied gate bias levels of about 1 V above threshold for an EOT of less than 1.4 nm.

[0003] One possible approach for decreasing EOT without increasing direct tunneling leakage current may involve substituting alternative oxides with dielectric constants ( $K$ ) that could exceed that of  $\text{SiO}_2$ . Silicon dioxide has a dielectric constant of approximately 3.9. For example, it may be desirable to obtain oxides with dielectric constants ranging from approximately 10 to more than 30. However, dielectric materials with higher values of  $K$  generally tend to have relatively small band gaps, which can also contribute to undesirable tunneling leakage current in semiconductor devices despite a relatively high dielectric constant.

[0004] Silicon nitride and silicon oxynitride alloys have been proposed as dielectric materials. Silicon nitride and silicone oxynitride alloys have dielectric constants of approximately 7.6 and 5.5 to 6.0 respectively. For example, C.J. Parker, G. Lucovsky and J.R. Hauser, *IEEE Electron. Device Lett.* (1998); Y. Wu and G. Lucovsky, *IEEE Electron. Device Lett.* (1998); and H. Yang and G. Lucovsky, *IEDM Digest*, (1999) propose oxide-nitride and oxide-oxynitride alloy stacked dielectrics with EOT projected to be greater than about 1.1 nm before tunneling leakage at approximately 1 V is increased above  $1\text{-}5\text{ A/cm}^2$ . The preparation of these stacked dielectrics proposes two  $300^\circ\text{C}$  remote plasma process steps: i) plasma-assisted oxidation to form Si-SiO<sub>2</sub> interface layers ranging in thickness from about 0.5 to 0.6 nm, and ii) remote plasma-enhanced chemical vapor deposition (RPECVD) to deposit either a nitride or an oxynitride (e.g.,  $(\text{SiO}_2)_x(\text{Si}_3\text{N}_4)_{1-x}$  with  $x \sim 0.5$ ) dielectric film in the dielectric stack. After deposition, a low thermal budget, e.g., 30 second,  $900^\circ\text{C}$ , rapid thermal anneal (RTA) has been proposed in an attempt to achieve chemical and structural relaxation. This RTA may promote optimized performance in IGFET devices [G. Lucovsky, A. Banerjee, B. Hinds, G. Clafflin, K. Koh and H. Yang, *J. Vac. Sci. Technol.* B15, 1074 (1997)]. Stacked nitride and oxynitride gate dielectrics may display improved performance and reliability with respect to thermally-grown oxides of the same EOT. Nonetheless, these gate dielectrics typically have EOT of greater than 1.1 nm in order to attempt to maintain direct tunneling leakage below  $1\text{ A/cm}^2$ . The nitride and oxynitride layers of these devices may be sufficiently thick to minimize or stop boron out-diffusion out of p<sup>+</sup> polycrystalline Si gate electrodes in the p-channel IGFETs [Y. Wu, et al., *Vac. Sci. Technol.* B17 1813 (1999)].

[0005] Other high-K dielectrics have been proposed (e.g., a K greater than 8) including TiO<sub>2</sub> [J. Yan, D.C. Gilmer, S.A. Campbell, W.L. Gladfelter and P.G. Schmid, *J. Vac. Sci. Technol.* B 14, 1706 (1996).], Ta<sub>2</sub>O<sub>5</sub> [H. Shinriki and M. Nakata, *IEEE Trans. on Elec. Devices* 38, 544 (1991)], Al<sub>2</sub>O<sub>3</sub> [L. Manchanda, W.H. Lee, J.E. Bower, F.H. Baumann, W.L. Brown, et al., *IEDM Tech. Dig.*, p. 605 (1998)], ZrO<sub>2</sub>, [R.B. van Dover, et al., *IEEE Electron Device Lett.*, 19, 329, (1998)] and Zr(Hf)O<sub>2</sub>-SiO<sub>2</sub> (also designated as Zr(Hf)-silicates; see van Dover et al.). These materials may not demonstrate the targeted goals of capacitance with decreased tunneling or leakage currents that may be desirable for silicon CMOS devices. For example, these materials may exhibit tunneling or leakage currents in CMOS devices

with EOT less than 1 nm. The performance of the materials may be limited due to the oxidation of the silicon substrate that can occur during thermal chemical vapor deposition (CVD) or during post-deposition processing, such as, for example, thermal anneals, to fully oxidize the deposited thin films.

[0006] Another high- $K$  dielectric is non-crystalline  $\text{Al}_2\text{O}_3$ . The dielectric constant of  $\text{Al}_2\text{O}_3$  is generally at most nine, but  $\text{Al}_2\text{O}_3$  has a band gap of more than 7 eV and conduction and valence band offset energies greater than 2 eV. However, because of its increased bond-ionicity with respect to  $\text{SiO}_2$  (Lucovsky, JVST), non-crystalline  $\text{Al}_2\text{O}_3$  dielectric films may display a high value of interfacial fixed negative charge, e.g., greater than  $10^{12} \text{ cm}^{-2}$ , as compared to less than  $10^{11} \text{ cm}^{-2}$  for  $\text{SiO}_2$  dielectrics, at interfaces with Si, or at interfaces with superficially thin ( $<0.5\text{-}1.0 \text{ nm}$ ) non-crystalline  $\text{SiO}_2$  in contact with Si. This high value of fixed charge has been correlated with electron and hole mobility degradation in the channel of IGFET devices and can contribute to reduced dimensionally scaled drive current potentially by factors of two or more. Accordingly, the gains in device capacitance derived from the increased value of  $K$  may be diminished.

[0007] Other relatively high- $K$  materials include transition metal and rare earth elemental oxides. These dielectrics may be qualitatively different than non-crystalline  $\text{SiO}_2$  and  $\text{Al}_2\text{O}_3$  in as much as the lowest conduction band states may be associated with localized atomic d-states of the respectively transition metal and rare earth atoms in marked contrast to the delocalized or extended s-state conduction band edge states of non-crystalline  $\text{SiO}_2$ ,  $\text{Al}_2\text{O}_3$  and the like. A comparison of an electronic structure diagram of the conduction band edge states of non-crystalline  $\text{SiO}_2$  and a metal or rare earth oxide is shown in **Figure 1**. Excitations to these states may show strong final state effects. Moreover, the lowest conduction band states may display a linear scaling of the optical band gap (the energy associated with the generation of a electron-hole pair created by absorption of a photon) with the atomic d-state energy in a configuration appropriate to bonding to oxygen atoms in a dielectric. For dielectric applications, this configuration is generally designated as  $s^2d^{n-2}$ , where  $n$  is total number of valence electrons. For example,  $n$  is 3 for the group IIIB transition metal atoms, and the lanthanide rare earth atoms, 4 for the group IVB transition metal atoms, and 5 for the group VB transition metal atoms. This scaling is displayed in **Figure 2**, where specific transition metal and rare earth oxides have been identified in the diagram. **Figure 2** also includes estimated and/or measured values of the

conduction band offset energies relative to Si. As noted above, there is also an empirical relationship between  $E_g$  and  $K$ , with  $E_g$  decreasing as  $K$  increases. Based on the experimental validation of the scaling in **Figure 1**, this scaling may eliminate several high- $K$  thin film dielectrics, including  $\text{TiO}_2$ ,  $\text{Nb}_2\text{O}_3$  and  $\text{Ta}_2\text{O}_3$  from incorporation into Si MOSFET devices.

**[0008]** There may be other problems in the application of elemental oxides, such as the transition metal oxides,  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{La}_2\text{O}_3$ , and the rare earth oxides including  $\text{Gd}_2\text{O}_3$  and the like, into aggressively scaled miniaturized MOSFET devices. The various problems that can be experienced include i) high values of interfacial fixed charge that are generally positive ii) ion and atom transport, iii) high reactivity with ambient gases, giving rise to incorporation of water or hydroxyl groups, and iv) lower than anticipated tunneling currents due to reduced electron masses associated with the electronic structure, e.g., the lowest conduction band have d-state properties. This last effect may be more apparent in transition metal oxides than in rare earth oxides. Other process integration issues may relate to the combined effects of their hydrophilic nature and oxygen ion transport that can promote changes in interface bonding during post-deposition thermal process steps, including dopant activation of atoms in source and drain contact to the channel in a MOSFET device.

**[0009]** Other high- $K$  dielectric materials include non-crystalline silicate and aluminate alloys, which are generally non-stoichiometric and may not correspond to the composition of a particular crystalline phase. For example, Hf silicate and aluminate alloys in the alloy composition range from ~25% to at most 50%  $\text{HfO}_2$  have been proposed, as well as Zr silicate and aluminate alloys. Hf silicates may have reduced reactivity with Si substrates and the like. However, one drawback for both group IVB silicates may be their thermal stability against chemical phase separation into  $\text{ZrO}_2$  or  $\text{HfO}_2$ , and a relatively low content silicate alloy (less than 10%  $\text{ZrO}_2$  or  $\text{HfO}_2$  as determined by the concentration of the eutectic in the equilibrium phase diagram), and crystallization of the  $\text{ZrO}_2$  or  $\text{HfO}_2$  phase. Thermal instability generally occurs at temperatures of ~ 900 °C for low  $\text{ZrO}_2$  content Zr silicate alloys, and at temperature ~ 1000 °C for low  $\text{HfO}_2$  content Hf silicates. Less is understood about chemical phase separation in aluminate alloys; however, there is some evidence for crystallization in Hf aluminate alloys. Decreases in  $K$  upon alloying with either  $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$  may be significant. For example, the Zr and Hf silicate alloys that display



the greatest amount of thermal stability against crystallization have dielectric constants less than 15. None-the-less they display reduced direct tunneling with respect to their respective end-member elemental oxides because of mitigating factors that increase as the transition metal oxide fraction increases, specifically the tunneling effective mass. The precursor bonding states that drive the chemical phase separation can be a function of the degree of rigidity or over-constrained bonding in the non-crystalline alloy, particularly in the composition range of about 25 to 50%  $\text{ZrO}_2$  or  $\text{HfO}_2$ . The increased rigidity of these alloys relative to non-crystalline  $\text{SiO}_2$ , and nano- or micro-crystalline  $\text{ZrO}_2$  or  $\text{HfO}_2$ , is the driving force for the chemical separation, e.g., the separated state is lower in energy, but also has a significantly reduced dielectric constant that renders phase separated dielectrics not useful for certain applications. In addition, the rigidity of these low  $\text{ZrO}_2/\text{HfO}_2$  content silicate films may result in i) defects in the bulk of the film that cannot be compensated by hydrogen or deuterium, and leads to electron injection and trapping under biased conditions, and also ii) defect formation at the semiconductor dielectric interfaces, e.g., Si atom dangling bonds in the strained Si in contact with the dielectric film, and/or a superficially thin region with predominantly Si-O bonding.

[0010] Other potential problems encountered with various high-K dielectrics may relate to: (1) the crystallization of the deposited films during either deposition or post-deposition processing, (2) the low dielectric constants of the bulk films that may be insufficient to meet the targeted goals, and (3) the formation of interfacial silicon oxides, or low content silicon oxide alloys (e.g., silicates) that may limit the attainable effective values of the K for the resulting stacked dielectric structure. For example, it is believed that oxidation of the silicon substrate during deposition or post-deposition processing may mitigate many of the gains of high-K layers with respect to achievable capacitance, whereas crystallization has the potential to open up alternative conduction pathways, the possibility of anisotropic dielectric constant behavior, and the potential to produce surface roughening.

[0011] The formation of interfacial silicide bonds may result in undesirable interfacial defects. Such defects may occur in the form of fixed positive charge or interface traps. Thus, it may be desirable to employ a thin dielectric interface layer of  $\text{SiO}_2$  between the dielectric layer and the silicon substrate. Utilizing such interfacial layers with known insulating film dielectrics, however, may be disadvantageous in that they may limit the dielectric stacks from having sufficient capacitance to meet the

ever-increasing scaling demands of CMOS devices. Additionally, this use of interfacial layers may also limit the incorporation of high-K oxides into devices that employ semiconductor substrates other than silicon such as, for example, silicon carbide, gallium nitride and compound semiconductors such as SiC, GaN, (Al,Ga)N, GaAs, (Al,Ga)As, (In,Ga)As, GaSb, (Al,Ga)Sb, (In,Ga)Sb, as well as nitride, arsenide and antimonide quaternary III-V alloys.

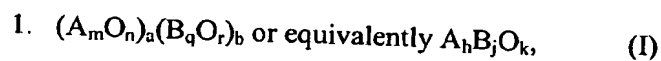
#### Brief Description of the Drawings

- [0012] **Figure 1** is an electronic structure diagram of band edge electronic states in SiO<sub>2</sub>, a representative network non-crystalline dielectric, and a thin film transition metal or rare earth oxide, representative of a large class of high-K elemental oxide dielectrics;
- [0013] **Figure 2** is a graph of the band gap and conduction band offset energy scaling for transition metal oxides as a function of the energy of their atomic highest occupied atomic d-state in the  $s^2d^{n-2}$  configuration;
- [0014] **Figures 3a and 3b** are cross sectional side views of a field effect transistor comprising a thin film oxide gate insulating layer according to embodiments of the present invention;
- [0015] **Figures 4a and 4b** are cross sectional side views of a photovoltaic device comprising a thin film oxide passivation layer according to embodiments of the present invention;
- [0016] **Figures 5a and 5b** are cross sectional side views of a high electron mobility transistor comprising a thin film oxide passivation layer according to embodiments of the present invention;
- [0017] **Figures 6a to 6d** are schematic illustrations of local bonding arrangements of the constituent atoms, including band edge electronic structures: **Figure 6a** illustrates silicon and aluminum oxides, SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>, respectively; **Figure 6b** illustrates elemental transition metal or lanthanide rare earth oxides; **Figure 6c** illustrates Tm or Re silicate or aluminate alloys, and **Figure 6d** illustrates complex oxides.
- [0018] **Figure 7** includes a schematic comparison of the band edge electronic structure non-crystalline Tm or Re elemental oxides, and non-crystalline complex oxide.

### Detailed Description

[0019] The present invention now will be described more fully hereinafter with reference to the accompanying drawings and examples, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

[0020] According to embodiments of the present invention, oxides are provided represented by the formula (I):



in which the elemental oxide components,  $A_mO_n$  and  $B_qO_r$ , are combined so that  $h = j$  or, equivalently  $ma = bq$ .  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers, and  $A$  is a lanthanide rare earth atom and  $B$  is a first, second or third row transition metal from group IIIB, IVB or VB, respectively. Oxides according to embodiments of the present invention include stoichiometric, single phase, complex oxides according to formula (I).

[0021] Referring to formula (I) and without wishing to be bound by theory, atoms  $A$  and  $B$  may have different respective atomic d-state energies in the  $s^2d^{n-2}$  configuration identified above. Examples of thin film complex oxides that are described by formula (I) include,  $GdScO_3$ ,  $Dy_2Ti_2O_7$ ,  $SmNbO_8$ , where  $Gd, Dy$ , and  $Sm$  are the  $A$  atoms are from the lanthanide rare earth group, and  $Sc, Ti$  and  $Nb$  are first row transition atoms from groups IIIB, IVB and VB, respectively. Accordingly, bonding arrangements may be specified at the atomic scale in stoichiometric thin film complex oxides according to embodiments of the present invention.

[0022] Moreover, separate and independent control may be provided with respect to i) electronic and optical band gaps, ii) conduction band offset energies with respect to semiconductors, including  $Si, Si, Ge$  alloys,  $Ge$ , as well as compound

semiconductors including SiC, GaN, (Al,Ga)N, GaAs, (Al,Ga)As, (In,Ga)As, GaSb, (Al,Ga)Sb, (In,Ga)Sb and the like, as well nitride, arsenide and antimonide quaternary III-V alloys, and iii) static dielectric constants. This can be accomplished through materials engineering at the atomic scale, and in particular through the interactions between the atomic d-states of the respective transition metal and rare earth atoms through bonding to a common bridging oxygen atom of the intrinsic microscopic bonding structures of these thin film, stoichiometric complex oxides. Thin film, stoichiometric complex oxides according to formula (I) may be integrated into metal-oxide-semiconductor (MOS) devices and can provide improved performance with respect to their constituent elemental oxides, and pseudo-binary alloys of their constituent oxides with network forming oxides such as non-crystalline SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> and the like. The complex oxides of this invention also provide surface passivation for photovoltaic devices, and buried channel high electron mobility transistors (HEMTs).

[0023] Complex oxides comprising group IIIB oxides such Y<sub>2</sub>O<sub>3</sub> and La<sub>2</sub>O<sub>3</sub> in combination with lanthanide rare earth oxides such as Gd<sub>2</sub>O<sub>3</sub> and the like may have different, potentially advantageous, properties when compared to their constituent elemental oxides. The complex oxides can be less hygroscopic in combination than their respective constituent oxides, which can result in advantages in processing complexity. This may be achieved while maintaining large band gaps, e.g., greater than about 5.5 eV and large conduction band offset energies, e.g., greater than 1.5 eV.

[0024] According to embodiments of the present invention, thin film gate dielectrics according to formula (I) can be provided that are a constituent of microelectronic devices such as insulating gate field effect transistors (IGFETs), that include crystalline, polycrystalline, and amorphous semiconductors. In still further embodiments according to the present invention, thin film surface passivation layer dielectric materials are provided for other devices including photovoltaics and buried channel field effect transistors, such as HEMTs. Thin film dielectrics according to embodiments of the present invention may be generally less than 150 nm thick, and may be non-crystalline as determined by conventional x-ray, electron or neutron diffraction, and electron imaging techniques, including, but not limited to high resolution transmission electron micrographs, in either the bright or dark field measurement configurations, or alternatively, and in both bright and dark field images of the same portion of the dielectric film. Moreover, high resolution analytical techniques that are incorporated in the scanning transmission electron microscopes

can be used to establish the single phase nature of dielectrics.

[0025] In some embodiments according to the present invention, thin film oxides according to formula (I) may be employed in field effect transistors as thin gate insulating layers having high dielectric constants. The thin film oxides potentially allow for field effect transistors employing the same to possess gate capacitance in excess of what may be achieved with conventional insulating layers and with reduced direct tunneling currents. As an example, the direct tunneling currents may be reduced by one order of magnitude, two to three orders of magnitude, or more from levels in excess of  $1 \text{ A/cm}^2$  for an EOT of approximately 1.5 to 1.6 nm.

[0026] The thin film oxides represented by formula (I) may also be employed as passivation or active layers in other electronic, photoelectronic and microelectronic devices, including, but not limited to high electron mobility transistors (HEMTs), and photovoltaic devices such as radiation detectors and solar energy converters.

[0027] Dielectric materials according to formula (I) may have applications in microelectronics and photovoltaic devices. For example, thin film dielectrics may be provided with high band gaps ( $E_g$ ), e.g., greater than 5 eV, and large conduction band offset energies in comparison to conventional semiconductor materials such as crystalline Si, e.g., greater than at least about 1 eV or about 1.5 eV and above. Dielectric materials according to Formula (I) may be used in i) metal-oxide semiconductor field-effect transistors (MOSFETs) or Si IGFETs, as well as ii) thin film transistors (TFTs), which include IGFETs in which all of the constituent layers are formed by thin film deposition techniques. Gate dielectrics according to formula (I) for silicon MOSFETs may have significantly higher dielectric constant ( $K$ ) than non-crystalline (or equivalently amorphous)  $\text{SiO}_2$  ( $K=3.9$ ) to enable the gate dielectric to reach an electrical equivalent of an  $\text{SiO}_2$  layer, generally designated as the equivalent oxide thickness or EOT, with a physical thickness,  $t_{\text{ox}}$ , of less than about 10 Å (See The International Technology Roadmap for Semiconductors: 1999 (Semiconductor Industry Association, San Jose, CA, 1999), pp. 105-141. and G.D. Wilk, R.M. Wallace, and J.M. Anthony, "High K Gate Dielectrics: Current Status and Materials Properties Considerations," J. Appl. Phys. 89 (2001) 5243-5275.) Moreover, gate dielectrics may be provided having a relatively large band gap of about 4 electron volts (eV), about 5 eV or more, and large band offset energies with respect to the conduction and valence bands of Si,  $\Delta E_c$  and  $\Delta E_v$ , respectively, at least ~1 eV or more than 1.5 eV in order to provide sufficiently low gate leakage.

[0028] According to some embodiments of the present invention, field effect transistors may be provided, including insulating gate field effect transistors (IGFETs), metal-oxide-semiconductor field effect transistors (MOSFETs) and thin film transistors (TFTs) that employ oxides represented by the formula (I). The field effect transistors comprise integrated circuit substrates having first surfaces, source and drain regions in the substrates at the first surfaces in spaced apart relationships, and gate insulating layers on the substrates at the first surfaces between the spaced apart source and drain regions. The gate insulating layers comprise the thin oxides represented by the formula (I). Source, drain, and gate contacts may be provided to contact the source and drain regions and the gate insulating layer, respectively.

[0029] Embodiments according to the present invention will be described in more detail with reference to the accompanying diagrams. Oxides represented by formula (I) may be used as dielectric material in integrated circuit devices, including very large scale integration (VLSI) devices including Insulated Gate Field Effect Transistors (IGFET), also referred to as MOSFET or CMOS devices. As an example, field effect transistors may be provided including gate insulators comprising non-crystalline oxides represented by the formula (I).

[0030] For the purposes of illustration, embodiments describing field effect transistors are set forth in **Figures 3a and b**. A field effect transistor **10** according to embodiments of the present invention is set forth in **Figure 3a**. The field effect transistor comprises an integrated circuit substrate **20** having a first surface **25**. Source and drain regions **30** and **40** respectively are present in the substrate **20** at the first surface **25** in a spaced apart relationship. A gate insulating layer **50** is present on the substrate **20** at the first surface **25** between the spaced apart source and drain regions, **30** and **40** respectively. The gate insulating layer **50** comprises the non-crystalline oxide represented by the formula (I) set forth herein. Source, drain, and gate contacts (**60**, **70**, and **80** respectively) are also present and contact source and drain regions **30** and **40** and the gate insulating layer **50**.

[0031] A number of materials can be employed in the integrated circuit substrate, the selection of which are known by those skilled in the art. As an example, the substrate may comprise a material selected from the group consisting of a Group III-V ternary alloy, a Group III-V quaternary alloy, a Group III-nitride alloy, and combinations thereof. Examples of Group III-V ternary alloys include, but are not limited to, (Ga,Al)As, (In,Ga)As, and combinations thereof. An example of a Group

III-V quaternary alloy includes, but is not limited to, (Ga,In)(As,P). Examples of Group III-nitride alloys include, but are not limited to, (Ga,Al)N, (Ga,In)N, (Al,In)N, (Ga,Al,In)N, and combinations thereof. Quaternary alloys of the above may also be employed. Additionally, group III-V antimonides, such as GaSb, III-V ternary antimonide alloys, (Al,Ga)Sb, (In,Ga)Sb, and III-V quaternary alloys, (In,Al,Ga)Sb are also included in MOSFET device substrates containing the channel region of the device.

[0032] Other examples of materials that may be employed in the integrated circuit substrate include, but are not limited to, silicon (Si), germanium (Ge), silicon carbide (SiC), gallium nitride (GaN), gallium arsenide (GaAs), as well as other compounds from Groups III and V. Combinations thereof may also be employed.

[0033] The integrated circuit substrate may encompass a number of specific substrates that are employed in devices of this type. One example of a substrate is a semiconductor-on-insulator (SOI) substrate.

[0034] The source, drain, and gate contacts may include those that are conventionally known in the art. As an example, the gate contact may be formed from polysilicon and/or metal materials.

[0035] The field effect transistor may also include other layers of materials. For example, in one embodiment (not shown), the field effect transistor may include an interfacial layer positioned between the substrate and the gate insulating layer. The interfacial layer may comprise an oxide. Other insulating materials may be employed. The interfacial layer may comprise silicon dioxide (SiO<sub>2</sub>), for example, in the event that the substrate comprises Si or SiC. Other interfacial layers such as those comprising gallium oxide (GaO<sub>3</sub>), aluminum oxide (Al<sub>2</sub>O<sub>3</sub>), or alloys thereof, may be used with compounds from Groups III and V along with their alloys. The use of the interfacial layer may be advantageous in electron-channel (n-channel) FETs and hole-channel (p-channel) FETs. The interfacial layer may contribute less than 0.5 nm of oxide-equivalent capacitance to the field effect transistor. In general, the use of an interfacial layer is believed to be advantageous in that it may: (1) prevent or minimize further oxidation of the silicon substrate during film deposition in highly oxidizing environments, (2) prevent or minimize formation of silicide bonds during the initial stages of deposition of the non-crystalline oxide materials, particularly with respect to, for example, the formation of Ta-Si bonds during the deposition of AlTaO<sub>4</sub>.

[0036] Referring now to **Figure 3b**, an additional layer 55 is depicted between the gate insulating layer 50 and the integrated circuit substrate 20 in field effect transistor 10. As shown in **Figure 3b**, the additional layer is in the form of a nitrided monolayer, the selection of which is known in the art.

[0037] The field effect transistor described herein may be fabricated by methods known to a person skilled in the art. For example, a gate insulating layer may be formed by depositing a non-crystalline oxide on the substrate of the field effect transistor by employing an appropriate technique including, but not limited to, those described herein. An interfacial layer may be formed on a substrate of the field effect transistor by a suitable process such as, but not limited to, remote plasma-assisted oxidation, low pressure thermal oxidation, chemical oxidation, or photo-assisted oxidation. Thereafter, the gate insulating layer is formed by depositing the non-crystalline oxide material on the interfacial layer in the same deposition chamber used to form the interfacial layer. Alternatively, an in-line system with substrate transfer in either a high vacuum or inert environment can be used, in which chemical reactions with the interfacial layer may be minimized or prevented.

[0038] As described herein, in various embodiments, the non-crystalline oxides may be employed in field effect transistors as thin gate insulating layers having high dielectric constants. Advantageously, the non-crystalline oxides potentially allow for field effect transistors employing the same to possess gate capacitance in excess of what may possibly be achieved with conventional insulating layers with significantly reduced direct tunneling currents. As an example, the direct tunneling currents may be reduced from levels in excess of  $1 \text{ A/cm}^2$ .

[0039] **Figure 4a** illustrates a photovoltaic device 150 having a p-type semiconductor layer ohmic contact 102, a p-type layer 101, an n-type layer 100, a dielectric film surface passivation layer 104, a second dielectric layer 105 and ohmic contacts 103. A thin film stoichiometric oxide, such as an oxide according to the formula (I), is used as a surface passivation layer 104. The surface passivation layer 104 can reduce loss of photo-generated carriers in the n-type semiconductor layer 100 of the device 150. The surface passivation layer 104 and the second dielectric layer 105 can together form an anti reflection coating. Dielectric thin films, such as oxides according to the formula (I), used as the surface passivation layer 104 may have positive fixed charge at the interface between the n-type layer 100 and the surface passivation layer 104. This may produce a surface potential at the interface that can



reduce recombination of photo-generated holes. Using the device 150 as a radiation detector under reverse bias (*i.e.*, with a positive bias applied to the n-layer 100 through the ohmic contact 103, and the p-layer 101 maintained at ground potential through the p-type semiconductor layer ohmic contact 102) it may be necessary to have holes generated by absorption of electromagnetic radiation in the infra red, visible or near ultra-violet regions of the spectrum be transmitted into the p-layer 101 and subsequently contribute to a short circuit current in the reverse bias mode. The device 150 can also be operated an open circuit voltage or the photo-diode detector mode when the ohmic contact 103 is connected to ground through a high impedance resistive load, or a power transfer mode when the impedance of the device 150 is matched to the load resistor and no additional bias is applied. As shown in Figure 4a, the passivation layer 104 can also serve as anti-reflection film through the incorporation of second dielectric 105, such as  $\text{Si}_3\text{N}_4$  or  $\text{SiO}_2$ , and the like. The second dielectric 105 can be thicker than the passivation layer 104, and the thickness may be tuned to a wavelength that is within the absorption band of the semiconductor materials that comprise n-type layer 100 and p-type layer 101, as for example, Si, (Si,Ge), Ge, SiC, GaAs, (Al,Ga)As, GaN, (In,Ga)N and the like.

[0040] As illustrated in Figure 4b, a third dielectric layer 106 has been added between the surface passivation layer 104 and the second dielectric layer 105, which are on p-type layer 110 and n-type layer 111. The conductivity types of layers 100 and 101 in Figure 4a and layers 110 and 111 in Figure 4b may be reversed so that the layers are complementary, *e.g.*, such that one is doped n-type and the other is doped p-type. The various dielectric layers, including the dielectric film surface passivation layer 104, the second dielectric layer 105, and the third dielectric layer 106, can be thin film, stoichiometry, single phase dielectrics, such as oxides of formula (I). Such dielectric materials generally have positive fixed charge. If the conductivity types are as shown in Figure 4b (*i.e.*, p-type semiconductor layer 110 and n-type semiconductor layer 111), then the third dielectric layer 106 may be inserted between the dielectric surface passivation layer 104 and the second dielectric layer 105. If the third dielectric layer 106 is  $\text{Al}_2\text{O}_3$ , and an alloy of  $\text{Al}_2\text{O}_3$  with  $\text{SiO}_2$ , then it may have negative fixed charge at the internal interface between the dielectric surface passivation layer 104 and the third dielectric 106. This configuration may reduce electron recombination at the surface of p-type semiconductor layer 110, and can improve device performance in any one the three modes of operation described

above. Moreover, the relative thicknesses of the dielectric layers including the dielectric surface passivation layer 104, the second passivation layer 105 and the third passivation layer 106 can be adjusted so that in combination they serve as anti reflection coating with respect to a wavelength of electromagnetic radiation that is consistent with a desired functionality of the device 150. The selection of relative thicknesses can be achieved through methods known to those of skill in the art.

[0041] A high electron mobility transistor or HEMT device 250 is shown in Figure 5a. The HEMT device 250 includes a substrate 203. Various layers of the HEMT device 250 are formed on the substrate 203, including a buried channel semiconductor layer 202, a wide band gap semiconductor confinement layer 201, a second wide band gap semiconductor confinement layer 203, an n-type source 208, an n-type drain 211, a gate electrode 205, a source electrode 207, and a drain electrode 210. An ohmic contact 209 to the substrate 203 and an ohmic contact 206 to the gate electrode 205 are provided. A passivation layer 204 between the n-type drain 211 and the gate electrode 205 and also between the n-type source 208 and the gate electrode 205 is provided. The passivation layer 204 can comprise a dielectric material, such as materials according to the formula (I). The passivation layer 204 can be a thin film, stoichiometric, single phase complex oxides.

[0042] In operation, a positive bias can be applied to the gate electrode 205, through the ohmic contact 206, and the source contact 207 can be held at ground potential through the source electrode 207, which is likewise grounded. A drain contact can be held at a positive potential through application of positive drain bias voltage to the drain electrode 210. The passivation layer 204 can suppress recombination of electrons at the respective portions of surface of the wide band gap semiconductor confinement layer 201, denoted as 201a and 201b, between the source 208 and the drain 211, and the gate electrode 205.

[0043] The semiconductor substrate 203, the wide band gap semiconductor confinement layer 201, the buried channel semiconductor layer 202, and certain other layers shown in Figure 5a can be made of various materials, the selection of which is known to those of skill in the art. For example, the substrate 203 and wide band gap semiconductor confinement layer 201 may be doped n-type Si, and the buried channel semiconductor layer 202 can be an undoped Si<sub>0.5</sub>Ge<sub>0.5</sub> alloy layer. Moreover, the source contact 208 and the drain contact 211 may be heavily doped, e.g.,  $>10^{19} \text{ cm}^{-3}$  n-type Si.

[0044] Alternatively, the semiconductor substrate 203 and wide band gap semiconductor confinement layer 201 may be doped n-type (In,Ga)As or other group III-V alloy semiconductors that can lattice-matched to an InP substrate, and the buried channel semiconductor layer 202 can be an undoped (In,Ga)As alloy layer with approximately 20 percent InAs content. The source contact 208 and the drain contact 211 may be a heavily doped ( $>10^{19} \text{ cm}^{-3}$ ) n-type (In,Ga)As alloy.

[0045] As another example, the semiconductor substrate 203 in contact with the buried channel semiconductor layer 202 and the wide band gap semiconductor confinement layer 201 may comprise a doped n-type (In,Ga)As alloy or other alloy semiconductors that are lattice matched to an InP substrate. The buried channel semiconductor layer 202 can be an undoped (In,Ga)As alloy layer with approximately 20 percent InAs content. The source contact 208 and the drain contact 211 can be heavily doped ( $>10^{19} \text{ cm}^{-3}$ ) n-type (In,Ga)As. The substrate 203 may also include an additional semiconductor layer (not shown), such as heavily doped InP that may be in contact with both the doped (In,Ga)As portion of 203, and the substrate layer ohmic contact 209.

[0046] In still another example, the semiconductor substrate 203 and the wide band gap semiconductor confinement layer 201 can be a doped n-type (Al,Ga)N alloy, and the buried channel semiconductor layer 202 can be an undoped (Al,Ga)N alloy or GaN. The source contact 208 and the drain contacts 211 can be heavily doped ( $>10^{19} \text{ cm}^{-3}$ ) n-type (Al,Ga)N. The substrate 203 may be a composite layer in which a portion of the substrate 203 adjacent the buried channel semiconductor layer 202 is doped n-type (Al,Ga)N, and a portion of the substrate layer 203 adjacent the substrate ohmic contact 209 is a single or composite semiconductor layer such as GaN or SiC, or a combination thereof. Alternatively, the portion of the substrate layer adjacent the substrate ohmic contact 209 may include an insulating substrate such as single crystal sapphire, e.g.,  $\text{Al}_2\text{O}_3$ .

[0047] Referring to Figure 5b, the device 250 further includes a second dielectric layer 212 that is placed between the passivation layer 204 and the gate electrode 205 and a portion of the side band gap semiconductor confinement layer 201. The second dielectric layer can be a dielectric material according to formula (I), or a stacked semiconductor layer comprising either thermally grown, or plasma oxidized native oxide such as silicon oxide, gallium oxide or aluminum oxide according, the selections of which are known to those skilled in the art.

[0048] HEMT devices according to embodiments of the present invention may include additional semiconductor layers for improved operation, and/or as may be required for epitaxial growth of the channel structures. The integration of and functionality of these passivation layers may be used in devices described with respect to the examples discussed herein. Additional passivation layers may be fabricated from other generic families of III-V semiconductors including antimonides such as GaSb, III-V ternary antimonide alloys, (Al,Ga)Sb, (In,Ga)Sb, and III-V quaternary alloys, (In,Al,Ga)Sb and the like.

[0049] According to embodiments of the present invention, the thin film, stoichiometric, single phase complex oxides, such as oxides described by formula (I), may be provided. Such oxides may have applications that include gate dielectrics and passivation layers for electronic and photonic devices as described herein. Oxide films may be provided that are generally thinner than 150 nm. The thickness of a film can be determined from cross section transmission electron micrographs or by spectroscopic techniques such as thin film interference, and spectroscopic or single wave length ellipsometry. Other methods may also be applied. Single phase, thin film complex oxides may be provided that can be either non-crystalline (as determined by conventional x-ray or electron diffraction methods, including bright field-dark field imaging, or alternatively nano- or micro-crystalline according to conventional diffraction methods indicated above, but also including other methods such as extended x-ray absorption fine structure spectroscopy, or EXAFS).

[0050] With reference to formula (I), A is a lanthanide rare earth atom and B is a first, second or third row transition metal from group IIIB, IVB or VB, respectively, that are bound to a common oxygen atom. Atoms A and B generally have different atomic d-state energies in the  $s^2d^{n-2}$  configuration. Without wishing to be bound by theory, the limitation for a specific type of stoichiometry, such as defined in formula (I), may result in coupling of both constituent atom atomic-d states through bonding to a common oxygen atom. The limitation may also exclude other possible bonding arrangements in which equal numbers of atoms of a given class, lanthanide rare earth or transition metal, are connected through a common oxygen atom. As one example, this may be achieved in chemically-ordered oxides, which include equal concentrations of these two metal atom constituents, the transition metal and lanthanide rare earth atoms, and in which the oxygen atom coordination is effectively even in character, e.g., four, six or eight, or a mixture thereof, and allowing for small

differences in nearest neighbor inter-atomic bond length that may be associated with the film morphology, non-crystalline, or micro- or nano-crystalline. Other bonding arrangements that involve bonding between oxygen atoms and the transition metal and lanthanide rare earth atoms are possible.

**[0051]** Without wishing to be bound by theory, a comparison between thin film stoichiometric complex oxides according to formula (I) and other high- $K$  dielectrics may be made with reference to the electronic structures illustrated in **Figures 6a to 6d**. **Figure 6a** is a schematic illustration of the basic element of local bonding, and the resultant band edge electronic structure in  $\text{SiO}_2$ . Similar bonding prevails in  $\text{Al}_2\text{O}_3$  as well. As shown in **Figure 6a**, the electronic structures consist of local arrangements in which Si and Al atoms, respectively, are connected as next-nearest bonding neighbors through a common oxygen atom. The electronic structure diagram indicates the chemical and symmetry character of the highest lying state in the valence band that determines, for example, the valence band offset energy difference with respect to crystalline Si, or to another semiconductor. This state is pure oxygen atom 2p non-bonding state with  $\pi$  symmetry. The lowest conduction band state is an anti-bonding silicon atom  $3s^*$ -state with  $\sigma$ -bonding character.

**[0052]** **Figure 6b** schematically illustrates the basic element of local bonding, and the resultant band edge electronic structure, in transition metal and lanthanide rare earth elemental oxides, e.g., the transition metal oxides  $\text{Y}_2\text{O}_3$ ,  $\text{ZrO}_2$  and  $\text{Nb}_2\text{O}_5$ , and the rare earth lanthanide trivalent oxides including, as an example,  $\text{Gd}_2\text{O}_3$ . The corresponding local bonding group includes transition metal or lanthanide rare earth atoms, denoted as Tm/Re as next nearest neighbors bonded to the same oxygen atom.

**[0053]** The highest lying states of the valence band are depicted in **Figure 6c**, which is a schematic illustration of the basic element of local bonding, and the resultant band edge electronic structure in transition metal (lanthanide rare earth) silicate and aluminate alloys in the low concentration alloy range. For these alloys there are three types of local bonding, denoted schematically as Si-O-Tm(Re), Si-O-Si and Tm(Re)-O-Tm(Re). The bonding arrangements vary with alloy content, and assuming chemically-ordered bonding at the compound silicate phase with the highest  $\text{SiO}_2$  concentrations corresponding to as examples,  $(\text{TmO}_2)_{0.5}(\text{SiO}_2)_{0.5}$  for group IVB Tm silicates where Tm = Zr and Hf, and  $(\text{Tm}_2\text{O}_3)_{0.33}(\text{SiO}_2)_{0.67}$  for group Tm (and also for trivalent lanthanide Re) silicates, in the concentration range from  $\text{SiO}_2$  to these compositions there are Si-O-Si and Si-O-Tm. For this alloy regime, which is may be

of interest for technology applications where Hf silicates are the materials of choice, the lowest conduction band states have been shown to be at the same energy relative to the conduction band of silicon as for  $\text{HfO}_2$  as represented schematically in a comparison between **Figures 6a to 6c**.

**[0054]** **Figure 6d** is a schematic illustration of the basic element of local bonding, and the resultant electronic structure the thin film, in stoichiometric complex oxides according to formula (I). For this case, atomic d-states of the respective Re and Tm with the same bonding symmetry, either  $\sigma$  or  $\pi$ , interact with each other through bonding to the same oxygen atom with a compatible bonding-symmetry, either  $\sigma$  or  $\pi$ , according the symmetry of the d-states, respectively,  $\sigma$  or  $\pi$ , in bonding groups represented schematically by Re-O-Tm. The resulting valence band states immediately below the top of the valence band defined by the oxygen 2p non-bonding p states, are energies that are different from those of Tm-O-Tm and Re-O-Re and complementary conduction states, particularly the state that the defines the lowest band gap, and the conduction band offset energy with respect to Si and other semiconductors is different as well.

**[0055]** Returning to **Figures 6a to 6c**, the band gaps and offset energies of the prior art gate dielectric and passivating oxides are discussed in more detail. The band gaps and band offset energies for the dielectrics of **Figure 6a** may result from bonding between atomic 3s and 3p states of Si or Al, and oxygen atom 2p states, and as such give rise to large band gaps, greater than 8 eV, intermediate range dielectric constants, here defined as being between 3.9 for  $\text{SiO}_2$  and at most 10-12, as well as relative large valence and conduction band offset energies greater than approximately 2 eV. The lowest conduction band states in  $\text{SiO}_2$  may be predominantly 3s-like, whereas, the lowest bonding states in  $\text{Al}_2\text{O}_3$  can include a larger mixing of 3p due to the increased bond ionicity, approximately 57% on the Pauling scale for  $\text{Al}_2\text{O}_3$  in contrast to ~45% on the same scale for  $\text{SiO}_2$ . The dielectrics having electronic states such as those shown in **Figure 6b** span a wide range of band gaps, dielectric constants and band offset energies where, as noted herein, and shown in **Figure 2**, the band gap and band offset energies can scale with the highest occupied atomic d-state energies of the respective transition metal and lanthanide rare earth lanthanide atoms in the  $s^2d^{n-2}$  configuration. There may also be an additional, but weaker scaling of the dielectric constant,  $K$ , with band gap;  $K$  typically increases as the band gap decreases. The situation for the silicate and aluminate alloys may be more complex, but

understood for dielectrics of according to the diagram of **Figure 6c**. The band gaps scale with alloy composition, increasing as either the  $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$  alloy fraction is increased, but the conduction band offset energies in the alloys with respect to Si and other semiconductors may be determined solely by the atomic d-state energies of the transition or rare earth atoms in much the same way as they are in the respective transition metal or rare earth elemental oxides. On the other hand the valence band offset energies with respect to Si and other semiconductors are increased as the  $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$  content can be increased.

[0056] Dielectrics according to the schematic diagram of **Figure 6d** may be qualitatively and quantitatively different than dielectric materials according to the schematic diagrams of **Figures 6a to 6c**. Because of d-state quantum mechanical wave function mixing through bonding of different transition metal and lanthanide rare earth atoms to a common oxygen atom, the valence band  $\pi$ -bonding states may be changed in energy, resulting in increases in both the band gaps of these complex stoichiometric oxides and their conduction band offset energies with respect to Si and other semiconductors. Choices of the different combinations of transition metal and rare earth atoms bonded to the same oxygen atom may effect the resulting properties of the material. For example, in general, the larger the difference in the atomic d-states of these atoms the larger the increase in band with respect to the smaller band gap member of the pair. As a general example, the lanthanide rare earth atomic 5d-state energies are nominally -5.6 to -6 eV with respect to vacuum; the lowest d-state energy if the -11 eV for the 3d state of Ti, with Nb and Ta following close behind with respective energies of -10 eV and -9.6 eV. Taking the 5d-state energy of an average lanthanide rare earth atom at -6.8 eV, the respective differences for a  $\text{ReTi}_2\text{O}_7$  complex oxide, a  $\text{ReNbO}_4$  complex oxide and a  $\text{ReTaO}_4$  complex oxides may be respectively, about 4.2 eV, 3.2 eV and 2.8 eV.

[0057] In some instances, the band gap shift can be estimated in context of a virtual crystal approximation such that the complex oxide displays properties that are a simple, or weighted averages of the end member oxides. Based on overlap integral differences, valence band states are at intermediate energies with respect to the corresponding elemental oxides states, thereby increasing the energy of the lowest conduction band state with respect to the transition metal oxide atom. An example of virtual crystal approximation scaling is illustrated by comparisons between  $\text{GdScO}_3$  and  $\text{ZrO}_2$ , where the onsets of strong absorption occur respectively at 5.8 and 5.7 eV,

demonstrating that that  $\text{GdScO}_3$  with 5d atomic states for the lanthanide rare earth atom Gd, and 3d atomic states for the transition metal atom Sc, has a band gap characteristic of a 4d transition metal oxide with a 4d-state energy equal to the average of the 3d- and 5d-state energies of Sc and Gd, respectively. The average atomic d-state energy in  $\text{GdScO}_3$ , equal to one-half of the sum of -6.6 eV for the 5d-state of Gd and -9.4 eV for the 3d-state of Sc equals -8 eV, which is approximately equal the atomic 4 d-state energy of Zr, -8.13 eV. The band edge electronic structure of a transition metal or rare earth elemental oxide, and a complex oxide according to formula (I), e.g., one comprised a group IIIB transition metal oxide such as  $\text{Sc}_2\text{O}_3$ , and lanthanide group rare earth oxide such as  $\text{Gd}_2\text{O}_3$ , is illustrated schematically in **Figure 7**. Specific examples of complex oxides identified by formula (I) include, but are not limited to thin film i)  $\text{GdScO}_3$ ,  $\text{DyScO}_3$ ,  $\text{SmScO}_3$ , and other trivalent lanthanide rare earth oxides in combination with the group IIIB transition metal oxide,  $\text{Sc}_2\text{O}_3$ , ii)  $\text{Gd}_2\text{Ti}_2\text{O}_7$ ,  $\text{Dy}_2\text{Ti}_2\text{O}_7$ ,  $\text{Sm}_2\text{Ti}_2\text{O}_7$  and other trivalent lanthanide rare earth oxides in combination with the group IVB transition metal oxide  $\text{TiO}_2$ , iii)  $\text{GdNbO}_4$ ,  $\text{DyNbO}_4$ ,  $\text{SmNbO}_4$  and other trivalent lanthanide rare earth oxides in combination with the group VB transition metal oxide  $\text{Nb}_2\text{O}_5$ , and iv)  $\text{GdTaO}_4$ ,  $\text{DyTaO}_4$ ,  $\text{SmTaO}_4$  and other trivalent lanthanide rare earth oxides in combination with the group VB transition metal oxide  $\text{Ta}_2\text{O}_5$ . As used herein, the lanthanide rare earth series is defined as it is in F.A. Cotton and G. Wilkenson, *Advanced Inorganic Chemistry, A Comprehensive Text*, 3rd Edition, (Interscience Publishers, New York, 1972), from Ce atomic number 58 with 1 4f electron, to Lu, atomic number 71 with a complete shell of 10 4f electrons. Accordingly, group IIIB elements are in order of increasing atomic number, Sc, atomic number 21, Y, atomic number 39, and La, atomic number 57.

**[0058]** Various tests may be used to characterize thin film oxides. One test involves studying the thin film sample by x-ray absorption spectroscopy, sometimes also called near edge x-ray absorption fine structure spectroscopy, either XAS, or NEXAFS, respectively. The specific test includes a study of three different absorptions which occur in 100 to 600 electron volt range of x-ray energies. Mono-energetic or monochromatic beams of x-rays in this energy range are readily available at synchrotron light sources at many different synchrotron sites, including Brookhaven National Laboratory and Stanford University in the United States, and these measurements can be performed at these or similar sites. The tests are described



by a specific example, and the extensions to other complex oxides are straightforward. For example, if the complex oxide is  $\text{GdScO}_3$ , the absorption spectrum can be plotted as normalized absorption in arbitrary units as a function of the photon energy of the X-rays in eV, for transitions from i) spin orbit split Sc 2p atomic states to symmetry split Sc 3d atomic states at a threshold of approximately 400 eV, ii) spin orbit split Gd 4p atomic states to symmetry split Gd 5d atomic states at a threshold of approximately 250 eV, and iii) the oxygen atom  $\text{K}_1$  edge with at a threshold energy of approximately 530 eV. A spectral width of interest for the Sc 2p transitions can be approximately 10 eV, for the Gd 4p transitions, or approximately 40 eV because of the larger spin orbit splitting,  $\sim 30$  eV in Gd as compared to 4-5 eV in Sc, and  $\sim 15$  eV for the O  $\text{K}_1$  edge. Two pairs of symmetry split transitions to 3d states may be observed for Sc, whereas these pairs of states may be evident, but not readily separable in the broadened 5d spectral features for Gd. As a result of the mixing, the complex oxide is expected to display evidence for no more than two d-states in the O  $\text{K}_1$  edge, a narrower one with more 3d character, and a broader one with more 5d character, and at an energy separation of approximately 3.5 to 4 eV. The occurrence of four d-state features in an O  $\text{K}_1$  spectrum, each mimicking what is observed in the oxygen  $\text{K}_1$  spectrum of the respective constituent oxides, may indicate that the material is not a chemically-ordered, stoichiometric complex oxides.

[0059] In addition to having band gaps and conduction band offset energies that may be increased as compared to the respective transition metal oxides,  $\text{Sc}_2\text{O}_3$ ,  $\text{TiO}_2$ ,  $\text{Nb}_2\text{O}_5$  and  $\text{Ta}_2\text{O}_5$ , oxides according to formula (I) may have relatively high values of  $K$ , e.g., intermediate between those of the respective transition metal and rare earth elemental oxides, but generally closer in value to those of the transition metal oxides.

[0060] Accordingly, various complex oxides may be provided that can have different properties compared with their elemental oxide constituents (e.g., oxides formed from either A or B in formula (I)). For example, certain elemental oxides may be strongly hydrophilic, such as can be characteristic of the lanthanide rare earth oxides. Certain elemental oxides may also display significant ionic conductivity, such as the group IVB oxides, most notably  $\text{ZrO}_2$ . In contrast, oxides according to formula (I) may result in reduced hydrophilic and ionic conductivity as compared with certain elemental oxides.

[0061] Methods of fabricating devices described herein can comprise delivering gaseous sources comprising element A, gaseous sources comprising element B, and

gaseous sources comprising oxygen on substrates such that the gaseous sources comprising element A, the gaseous sources comprising element B, and the gaseous sources comprising oxygen react to form the a desired complex oxide. The elements A and B are delivered in amounts necessary and sufficient for achieving chemical stoichiometry, e.g., equal concentrations of A and B atoms in the resulting thin films. The gaseous sources comprising oxygen can contain a sufficient amount of chemically active oxygen such that the elements A and B are completely oxidized. For example, the delivery of the gases may be carried out as a deposition. Various gaseous sources comprising element A and gaseous sources comprising element B may be employed. Examples of gaseous sources comprising element A and gaseous sources comprising element B include, but are not limited to, alkoxide compounds, organo-metallic compounds, inorganic compounds, and mixtures thereof. The alkoxide compound may be selected from the group consisting of an ethoxide, a propoxide, and a butoxide. Other gaseous sources comprising element A and gaseous sources comprising element B can be used, such as organo-metallic source gases, including those that are capable of producing the desired binary oxides (e.g., diketonates) along with other organo-metallics that contain metal-oxygen bonds. Other inorganic sources of elements A and B can be employed such as halides and nitrates. The gaseous sources comprising element A and/or element B can be derived through the evaporation of respective liquid sources comprising these elements, particularly in embodiments in which the deposition involves a physical deposition or a plasma chemical vapor deposition process.

[0062] A number of sources of oxygen may be employed. Exemplary sources of oxygen include, but are not limited to, oxygen atoms, oxygen ions, oxygen metastables, oxygen molecular ions, oxygen molecular metastables, compound oxygen molecular ions, compound oxygen metastables, compound oxygen radicals, and mixtures thereof. Compounds that can be employed in the gaseous sources include, but are not limited to,  $O_2$ ,  $N_2O$ , and mixtures thereof. The formation of thin film complex oxides may take place in non-equilibrium chemical environments.

[0063] The gaseous sources comprising element A, element B, and oxygen may further comprise other components such as, for example, inert gases (e.g., argon (Ar) helium (He), or other noble gases, as well as mixtures thereof).

[0064] A number of deposition techniques can be used in forming thin film oxides. Exemplary techniques include, but are not limited to, a laser-assisted chemical vapor

deposition, a direct or remote plasma assisted chemical vapor deposition, a electron cyclotron resonance chemical vapor deposition, a reactive physical vapor deposition and an atomic layer deposition. For example, a remote plasma assisted chemical deposition (REPCVD) can be employed. Various reactive physical vapor depositions can be used such as, for example, a thermal evaporation, an electron beam evaporation, a parallel plate radio frequency (rf) sputtering, a direct current (dc) sputtering, a radio frequency (rf) magnetron sputtering, and a direct current (dc) magnetron sputtering. A reactive physical vapor deposition may also occur in the form of an atomic layer absorption process.

[0065] Fabrication of thin films according to embodiments of the invention may be carried out under any number of temperature and pressure conditions. Various fabrication steps may be carried out at a temperature from about 250°C to about 400°C and or at pressure conditions from about 200 milli-Torr to about 500 milli-Torr.

[0066] Conventional equipment may be used to fabricate complex oxides, including, for example, a suitable reactor (e.g., reaction chamber or vessel). For example, alkoxide liquids comprising elements A and B may be injected into a reactor downstream from a remote radio-frequency excited plasma. The alkoxides may be liquids at room temperature, but at the temperature range employed in the reactor have sufficient levels of vapor to be transported into the reactor. A microwave plasma may be employed, if desired.

[0067] The gaseous source comprising oxygen may be plasma-excited, e.g., by being subjected to a radio-frequency or microwave-frequency source. The gaseous source comprising oxygen may be present in combination with an inert gas such as, for example, a rare gas such as, but not limited to, helium (He) or argon (Ar)). The gaseous source comprising oxygen may be injected into the reactor at a high flow rate (e.g., 200 standard cubic centimeter per second (SCCM) through a tube with an inside diameter of about one inch) through a plasma tube at a location upstream relative to where the gaseous source comprising element A and the gaseous source comprising element B are injected into the reactor. The above injection configuration is believed to be potentially advantageous since it may minimize back-streaming of the gaseous sources comprising element A and the gaseous sources comprising element B. See e.g., G. Lucovsky, *IBM J. of Res. and Devel.* 43, 301 (1999).

[0068] Other techniques can be employed to provide for the deposition of the thin film complex oxide materials in a highly oxidizing environment. Exemplary techniques include, but are not limited to, embodiments involving plasma deposition, such as direct plasma deposition in conventional parallel plate reactors, triode plasma deposition, electron-cyclotron-resonance plasma deposition, laser-assisted deposition, and reactive physical vapor deposition using ozone, plasma-excited oxygen, or laser excited oxygen.

[0069] Depending on the particular application, thin film dielectrics may be deposited onto either i) insulating substrates such as bulk fused silica and crystalline aluminum oxide (sapphire), ii) semiconductor substrates such as and not limited to Si, Ge, (Si,Ge) alloy, SiC, GaN, GaAs, GaSb, InP and other group III-V ternary and quaternary alloy substrates, ZnS, ZnSe, CdTe and group II-VI ternary and quaternary substrates, iii) semiconductor substrates with thin dielectric layers, including, but not restricted to Si with (a) nitrided SiO<sub>2</sub>, and (b) non-crystalline La aluminate, and (b) GaN and (Ga,Al)N and the like with GaO<sub>x</sub> or AlO<sub>x</sub>,  $x \sim 1.5$ , and iv) metallic substrates including ordinary metals such as Al and the like, transition metals and rare earths, including Ti, Ta, Mn, Fe, Co, and Ni, and lanthanide rare earth metals, including Gd, Nd and the like.

[0070] The depositions of the complex oxides may be performed in ultra-high-vacuum compatible multi-chamber systems equipped with conventional substrate introduction load locks, and the like, but they can also be performed in reactors that incorporate sufficient purging, and gas flow dynamics to prevent chemical contamination of films or substrates. Specific vacuum compatible deposition techniques include: i) chemical vapor deposition from organo-metallic, halide or hydride transition metal and rare earth precursor molecules in the presence of strong oxidizing agents such as oxygen atoms, ozone, or other oxide molecules that are known sources of oxygen, such as, and not limited to nitrous oxide, N<sub>2</sub>O and nitric oxide, NO, ii) plasma or photo-assisted chemical vapor deposition using the same transition metal, rare earth and oxygen atom precursor species as for chemical vapor deposition, iii) reactive physical vapor deposition from elemental or compound sources, iv) magnetron or parallel plate reactive sputtering from elemental or compound targets in an ambient that leads to formation of stoichiometric complex oxides, v) atomic layer deposition using precursor and oxidizing cycles that leads to formation of stoichiometric complex oxides.

[0071] Further embodiments according to the present invention are described in detail with reference to the non-limiting examples provided below.

#### EXAMPLE 1

[0072] A field effect transistor is formed according to the following procedure. Radio frequency remote plasma assisted oxidation using oxygen as the source gas is employed to form an  $\text{SiO}_2$  insulating layer on a Si-containing substrate such as Si, SiC or a (Si,Ge) alloy. The above process is carried out at  $300^\circ\text{C}$ . A thin film, stoichiometric, single phase complex oxide according to formula (I) is formed on the insulating layer via a radio frequency remote plasma enhanced CVD deposition carried out at  $300^\circ\text{C}$ . The structure is then exposed to a post deposition rapid thermal anneal in an inert, non-oxidizing ambient such as helium or argon for e.g., 30 seconds at  $900^\circ\text{C}$ .

[0073] The resulting field effect transistor has an  $\text{SiO}_2$  insulating layer with a thickness of less than 0.5 nm (i.e., 5 Å) and a gate insulating layer physical thickness of more than 2.0 nm (i.e., 20 Å), that, in combination with the interfacial  $\text{SiO}_2$  layer is chosen to meet the targeted EOT, e.g., in the range of 0.7 nm to 1.5 nm.

#### EXAMPLE 2

[0074] A field effect transistor is formed according to the procedure set forth in Example 1 with the following modifications. The substrate is exposed to an  $\text{N}_2$  remote plasma to allow for the formation of a nitrided monolayer on the substrate. The other layers are formed in the manner previously described.

#### EXAMPLE 3

[0075] A field effect transistor is formed according to the procedure set forth in Example 1 with the following modifications. A remote plasma assisted oxidation using  $\text{N}_2\text{O}$  instead of  $\text{O}_2$  is employed to form the nitrided monolayer thereon with the interfacial layer thereon.

#### EXAMPLE 4

[0076] The devices described in Examples 1, 2 and 3, wherein the Ge, (Si,Ge) alloys, GaN, (Al,Ga)N and (In,Ga)N and other compound III-V semiconductors alloys, such as GaAs, (Al,Ga)As, InP, (In,Ga)As and the like are substituted for c Si.

are employed as the semiconductor substrate layer which includes the channel. When compound III-V semiconductors other than GaN and (Al,GaN) or (In,Ga)N are used as the substrate, these substrate layers may include a sacrificial semiconductor layer such as Si or GaN nitride, adjusted in thickness to be converted to a silicon or gallium oxide during the oxidation steps of Examples 1, 2 and 3, and to prevent oxidation of the underlying substrates which could result in the formation of elemental arsenic or phosphorus, or their oxides.

#### EXAMPLE 5

[0077] A silicon based HEMT device, in which the channel layer is a (Si,Ge) alloy, the confining layers are Si, and in which the passivation layer covers the portions of the device between the source and gate electrode, and the drain and the gate electrode.

#### EXAMPLE 6

[0078] A silicon based HEMT device is provided, in which the channel layer is a (Si,Ge) alloy, the confining layers are Si, and in which the passivation layer covers the portions of the device between the source and gate electrode, and the drain and the gate electrode, and in which there is an additional interfacial oxide, or nitrided oxide layer that extends over the entire surface of the device, including the gate electrode region. The passivation layer covers this layer between the source and gate electrode, and the drain and the gate electrode, and the gate electrode covers this layer as well.

#### EXAMPLE 7

[0079] A HEMT device based on III-V alloys that are lattice matched to InP. This includes in one embodiment, an (In,Ga)As channel and confining and substrate lattice matched alloys that are also lattice matched to InP. The passivation layer comprises at least one constituent that is a thin film oxide according to formula (I), and covers the portions of the device between the source and gate electrode, and the drain and the gate electrode. In a second embodiment, the first constituent of the multi-layer passivation film, also extends below the gate electrode, and is covered completely by the gate electrode.

EXAMPLE 8

[0080] A HEMT device based on III-V alloys that are lattice matched to GaN. This can include a GaN channel and confining and substrate layers are lattice matched alloys with wider band gap, as (Al,Ga)N. The passivation layer comprises at least one constituent that is a thin film oxide according to formula (I), and covers the portions of the device between the source and gate electrode, and the drain and the gate electrode. Alternatively, the first constituent of the multi-layer passivation film, also extends below the gate electrode, and is covered completely by the gate electrode.

EXAMPLE 9

[0081] A HEMT device based on group III-V antimonides. This can includes a HEMT device in which a GaSb layer is the channel and confining and substrate layers, which are lattice matched alloys with wider band gap, as (Al,Ga)Sb. The passivation layer comprises at least one constituent according to formula (I), and covers the portions of the device between the source and gate electrode, and the drain and the gate electrode. In a second embodiment, the first constituent of the multi-layer passivation film, also extends below the gate electrode, and is covered completely by the gate electrode.

EXAMPLE 10

[0082] A first photovoltaic example in which the substrate material is doped n-type Si, either single crystal, polycrystalline or microcrystalline, and the top layer of the device is doped p-type Si, again either single crystal, polycrystalline or microcrystalline. An ohmic contact is made to the entire bottom surface of the substrate material, and the top surface ohmic contact is either in a ring geometry that is at the perimeter of a circular device, an inter-digitated or comb-like contact that is customized to the device geometry, e.g., either square or rectangular, or of another design that is consistent with maximizing the surface exposed to radiation, and minimizing any parasitic series resistance that derives from the limit coverage of the top surface. The same geometry can be employed with compound semiconductors, e.g., SiC, GaN, GaAs, InAs, and the like, and their ternary or quaternary alloys. The conductivity types of the top and substrate layers can also be reversed.

[0083] With respect to the above examples, the devices describe may include a

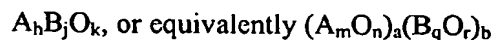
thin film, stoichiometric, single phase complex oxide according to formula (I) as one constituent of a surface passivation film. The surface passivation film layer may also provide an anti-reflection function as well. Various other dielectric components of semiconductor devices can be fabricated using the complex oxide according to formula (I), including a capacitor dielectric or an isolation trench.

**[0084]** In the drawings and specification, there have been disclosed embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation. The following claims are provided to ensure that the present application meets all statutory requirements as a priority application in all jurisdictions and shall not be construed as setting forth the scope of the present invention.



**THAT WHICH IS CLAIMED:**

1. A thin film, stoichiometric, single phase complex oxide represented by the formula



in which the elemental oxide components,  $(A_m O_n)$  and  $(B_q O_r)$  are combined so that  $h = j$  or, equivalently  $ma = bq$ , and  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers; and wherein:

A is an element selected from the lanthanide rare earth elements of the periodic table, the trivalent elements from cerium (Ce) to lutetium (Lu); and

B is an element selected from the transition metal elements of groups IIIB, IVB and VB of the periodic table.

2. An oxide according to Claim 1 wherein B is chosen from the group including group of IIIB, IVB and VB transition metals with 3d, 4d or 5d electrons available for bonding to oxygen, and where A is a lanthanide rare earth atom in which one 5d electron is available for bonding as in trivalent ions.

3. An oxide according to Claim 1, wherein B is either scandium (Sc), titanium (Ti), tantalum (Ta) or niobium (Nb), and where A is a lanthanide rare earth atom.

4. An oxide according to Claim 3, wherein A is either trivalent gadolinium (Gd), or praseodymium (Pr) or lutetium (Lu).

5. An oxide according to Claim 3, wherein A is the remainder of the trivalent lanthanide rare earth elements cerium (Ce), neodymium (Nd), promethium (Pm), samarium (Sm), europium (Eu), terbium (Tb), dysprosium (Dy), holmium (Hm), erbium (Er), thulium (Tm), and ytterbium (Yb).

6. A method of forming a thin film, stoichiometric, single phase complex oxide represented by the formula



in which the elemental oxide components,  $(A_mO_n)$  and  $(B_qO_r)$  are combined so that  $h = j$  or, equivalently  $ma = bq$ , and  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers; and

wherein:

A is an element selected from the lanthanide rare earth element of the periodic table, the trivalent elements from cerium (Ce) to lutetium (Lu); and

B is an element selected from the transition metal element of groups IIIB, IVB and VB of the periodic table; said method comprising:

delivering a gaseous source comprising element A, a gaseous source comprising element B, and a gaseous source comprising oxygen on a substrate such that the gaseous source comprising element A, the gaseous source comprising element B, and the gaseous source comprising oxygen react to form the non-crystalline oxide; and

7. The method according to Claim 6, wherein elements A and B are present in amounts sufficient to achieve chemical stoichiometry, and wherein the gaseous source comprising oxygen contains a sufficient amount of oxygen such that the elements A and B are completely oxidized.

8. A method according to Claim 6, wherein the oxygen in the gaseous source comprising oxygen-containing source is selected from the group consisting of oxygen atoms, oxygen ions, oxygen metastables, oxygen molecular ions, oxygen molecular metastables, compound oxygen molecular ions, compound oxygen metastables, compound oxygen radicals, and mixtures thereof.

9. A method according to Claim 6, wherein the gaseous source comprising oxygen comprises  $O_2$  or  $N_2O$ .

10. A method according to Claim 6, wherein said depositing step is a remote plasma-enhanced chemical vapor deposition occurring in a reactor, and wherein the remote-plasma-enhanced chemical vapor deposition comprises:

subjecting the gaseous source comprising oxygen to radio-frequency plasma-excitation or microwave frequency plasma-excitation, the gaseous source comprising oxygen further comprising a rare gas element;

wherein the gaseous oxygen-containing source is injected into the reactor upstream relative to the gaseous source comprising element A and the gaseous source comprising element B.

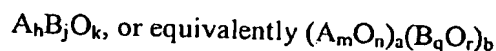
11. A method according to Claim 10, wherein the rare gas element is selected from the group consisting of argon (Ar) and helium (He).

12. A method according to Claim 6, wherein B is chosen from the group including group of IIIB, IVB and VB transition metals with 3d, 4d or 5d electrons available for bonding to oxygen, and where A is a lanthanide rare earth atom in which one 5d electron is available for bonding as in trivalent ions.

13. A method according to Claim 6, wherein B is either scandium (Sc), titanium (Ti), tantalum (Ta) or niobium (Nb), and where A is a lanthanide rare earth atom.

14. A method according to Claim 6, wherein the reactive physical deposition is an atomic layer absorption process, which includes a gate or passivation layer that comprises the complex oxide.

15. A field effect transistor comprising:  
an integrated circuit substrate having a first surface;  
source and drain regions in said substrate at said first surface in a spaced apart relationship;  
a gate insulating layer on said substrate at said first surface between said spaced apart source and drain regions, said gate insulating layer comprising a thin film complex oxide represented by the formula:



in which the elemental oxide components,  $(A_mO_n)$  and  $(B_qO_r)$  are combined so that  $h = j$  or, equivalently  $ma = bq$ , and  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers; and

wherein:

A is an element selected from the lanthanide rare earth elements of the periodic table, the trivalent elements from cerium (Ce) to lutetium (Lu);

B is an element selected from the transition metal elements of groups IIIB, IVB and VB of the periodic table;

and source, drain, and gate contacts that contact said source and drain regions and said gate insulating layer, respectively; and  
a gate on the gate insulating layer.

16. A field effect transistor according to Claim 15, wherein said substrate comprises a material selected from the group consisting of a Group III-V binary alloy, a Group III-V quaternary alloy, a Group III-nitride alloy, and combinations thereof.

17. A field effect transistor according to Claim 15, wherein the substrate comprises a Group III-V binary alloy selected from the group consisting of (Ga,Al)As, (In,Ga)As, and combinations thereof.

18. A field effect transistor according to Claim 15, wherein the substrate is a Group III-V quaternary alloy which is (Ga,In)(As,P).

19. A field effect transistor according to Claim 15, wherein the substrate is a Group III-nitride alloy selected from the group consisting of (Ga,Al)N, (Ga,In)N, (Al,In)N, (Ga,Al,In)N, and combinations thereof.

20. A field effect transistor according to Claim 15, wherein said substrate comprises a material selected from the group consisting of silicon (Si), germanium (Ge), silicon carbide (SiC), gallium nitride (GaN), gallium arsenide (GaAs), and combinations thereof.

21. A field effect transistor according to Claim 15, wherein said substrate is a semiconductor-on-insulator (SOI) substrate.

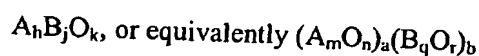
22. A field effect transistor according to Claim 15, further comprising an interfacial layer positioned between said integrated circuit substrate and said gate insulating layer.

23. A field effect transistor according to Claim 22, wherein said interfacial layer comprises silicon dioxide ( $\text{SiO}_2$ ).

24. A field effect transistor according to Claim 22, wherein the interfacial layer contributes less than about 0.5 nm of oxide-equivalent capacitance to said field effect transistor and is nitrided silicon dioxide layer.

25. A field effect transistor according to Claim 22, wherein the interfacial layer contributes less than about 0.5 nm of oxide-equivalent capacitance to said field effect transistor and includes  $\text{LaAlO}_3$ .

26. A photovoltaic device comprising a surface passivation layer, the surface passivation layer comprising a thin film, stoichiometric, single phase complex oxide represented by the formula



in which the elemental oxide components,  $(A_m O_n)$  and  $(B_q O_r)$  are combined so that  $h = j$  or, equivalently  $ma = bq$ , and  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers; and wherein:

A is an element selected from the lanthanide rare earth elements of the periodic table, the trivalent elements from cerium (Ce) to lutetium (Lu); and

B is an element selected from the transition metal elements of groups IIIB, IVB and VB of the periodic table.

27. A high electron mobility transistor device comprising a dielectric layer, the dielectric layer comprising a thin film, stoichiometric, single phase complex oxide represented by the formula



in which the elemental oxide components,  $(A_mO_n)$  and  $(B_qO_r)$  are combined so that  $h = j$  or, equivalently  $ma = bq$ , and  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers; and wherein:

A is an element selected from the lanthanide rare earth elements of the periodic table, the trivalent elements from cerium (Ce) to lutetium (Lu); and

B is an element selected from the transition metal elements of groups IIIB, IVB and VB of the periodic table.

28. A thin film, stoichiometric, single phase complex oxide represented by the formula



in which the elemental oxide components,  $(A_mO_n)$  and  $(B_qO_r)$  are combined so that  $h = j$  or, equivalently  $ma = bq$ , and  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers; and wherein:

A is an element selected from the lanthanide rare earth elements of the periodic table, the trivalent elements from cerium (Ce) to lutetium (Lu), wherein B is chosen from the group including group of IIIB, IVB and VB transition metals with 3d, 4d or 5d electrons available for bonding to oxygen; and

wherein the oxide is prepared by i) chemical vapor deposition from organo-metallic, halide or hydride transition metal and rare earth precursor molecules in the presence of strong oxidizing agents such as oxygen atoms, ozone, or other oxide molecules that are known sources of oxygen, such as, and not limited to nitrous oxide, N<sub>2</sub>O and nitric oxide, NO, ii) plasma or photo-assisted chemical vapor deposition using the same transition metal, rare earth and oxygen atom precursor species as for chemical vapor deposition, iii) reactive physical vapor deposition from elemental or compound sources, or iv) magnetron or parallel plate reactive sputtering from elemental or compound targets in an ambient that leads to formation of stoichiometric complex oxides, or v) atomic layer deposition using precursor and oxidizing cycles that leads to formation of stoichiometric complex oxides.

29. A thin film oxide according to Claim 28, is prepared by either i)

chemical vapor deposition from organo-metallic, halide or hydride transition metal and rare earth precursor molecules in the presence of strong oxidizing agents such as oxygen atoms, ozone, or other oxide molecules that are known sources of oxygen, such as, and not limited to nitrous oxide,  $N_2O$  and nitric oxide,  $NO$ , ii) plasma or photo-assisted chemical vapor deposition using the same transition metal, rare earth and oxygen atom precursor species as for chemical vapor deposition, iii) reactive physical vapor deposition from elemental or compound sources, iv) magnetron or parallel plate reactive sputtering from elemental or compound targets in an ambient that leads to formation of stoichiometric complex oxides, or v) atomic layer deposition using precursor and oxidizing cycles that leads to formation of stoichiometric complex oxides.

30. A thin film, stoichiometric, single phase complex oxide represented by the formula



in which the elemental oxide components,  $(A_mO_n)$  and  $(B_qO_r)$  are combined so that  $h = j$  or, equivalently  $ma = bq$ , and  $a, b, h, j, k, m, n, q$  and  $r$  are non-zero integers; and wherein:

A is an element selected from the lanthanide rare earth elements of the periodic table, the trivalent elements from cerium (Ce) to lutetium (Lu); and

B is an element selected from the transition metal elements of groups IIIB, IVB and VB of the periodic table;

wherein the oxide is prepared by either i) chemical vapor deposition from organo-metallic, halide or hydride transition metal and rare earth precursor molecules in the presence of strong oxidizing agents such as oxygen atoms, ozone, or other oxide molecules that are known sources of oxygen, such as, nitrous oxide,  $N_2O$  and nitric oxide,  $NO$ , ii) plasma or photo-assisted chemical vapor deposition using the same transition metal, rare earth and oxygen atom precursor species as for chemical vapor deposition, iii) reactive physical vapor deposition from elemental or compound sources, iv) magnetron or parallel plate reactive sputtering from elemental or compound targets in an ambient that leads to formation of stoichiometric complex oxides, or v) atomic layer deposition using precursor and oxidizing cycles that leads to formation of stoichiometric complex oxides.

## COMPLEX OXIDES FOR USE IN SEMICONDUCTOR DEVICES AND RELATED METHODS

### Abstract

Thin film, single phase, complex oxides comprising stoichiometric mixtures of different group IIIB, IVB and VB transition metal oxides, such as  $\text{Sc}_2\text{O}_3$ ,  $\text{TiO}_2$ , and  $\text{Nb}_2\text{O}_5$  or  $\text{Ta}_2\text{O}_5$  oxides, respectively, are combined with lanthanide group rare earth oxides such as  $\text{Gd}_2\text{O}_3$  and the like.



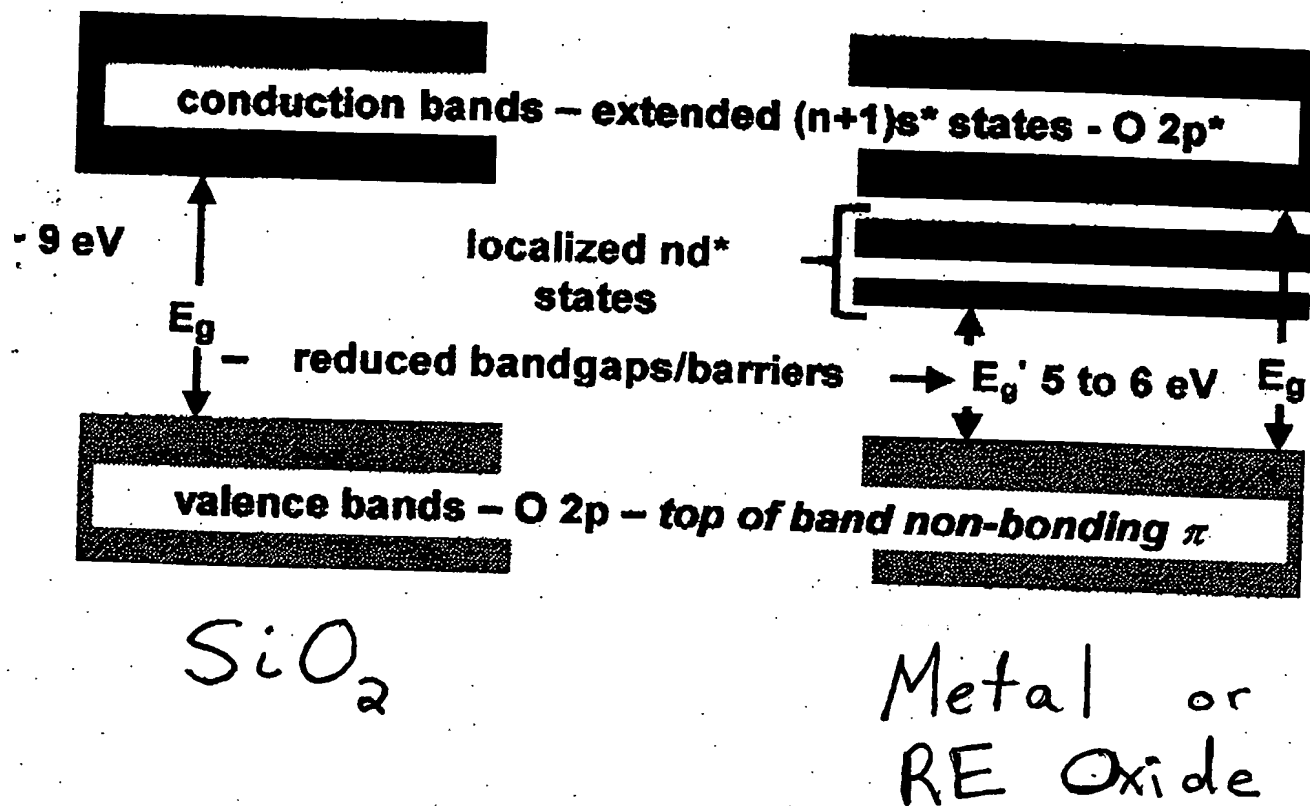


FIG. 1

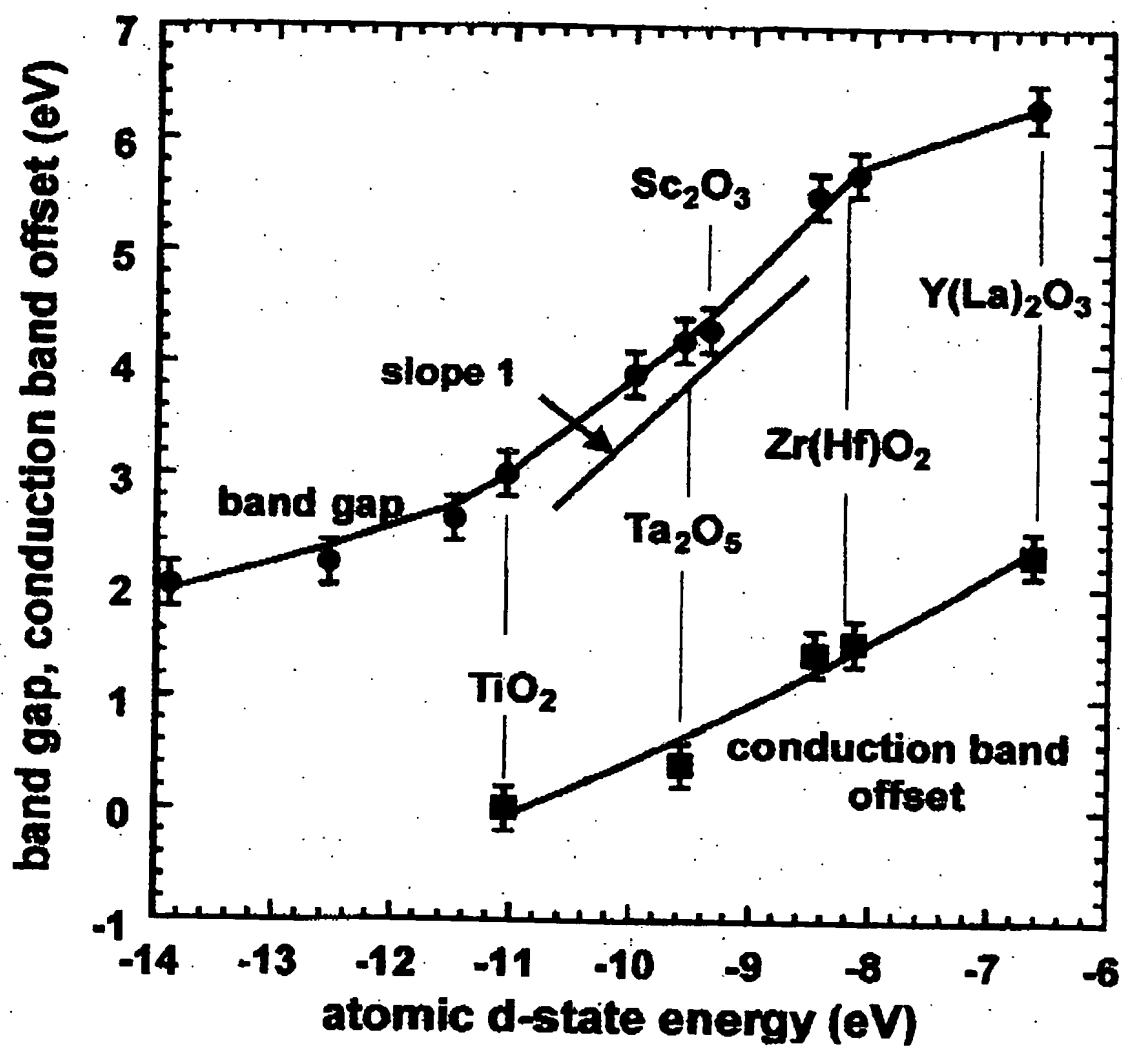


FIG. 2

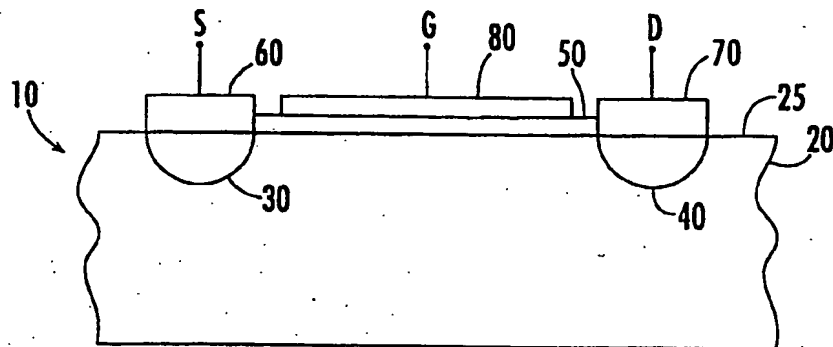


FIG. 3a

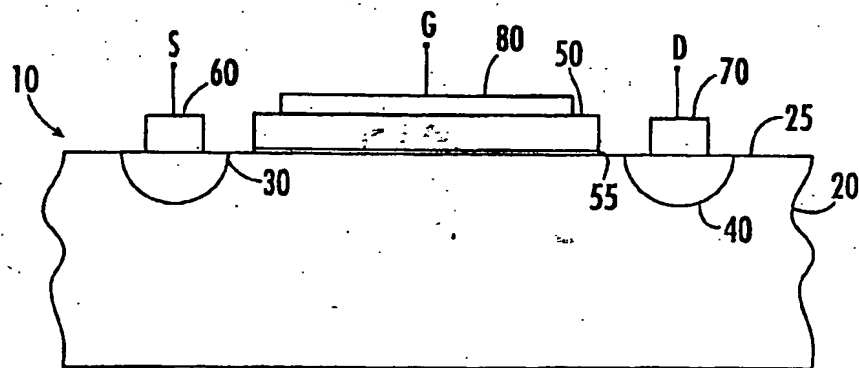


FIG. 3b

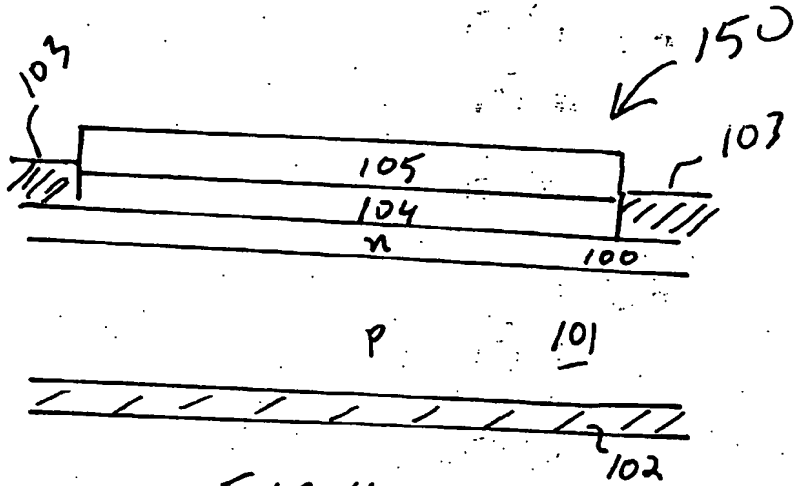


FIG. 4a

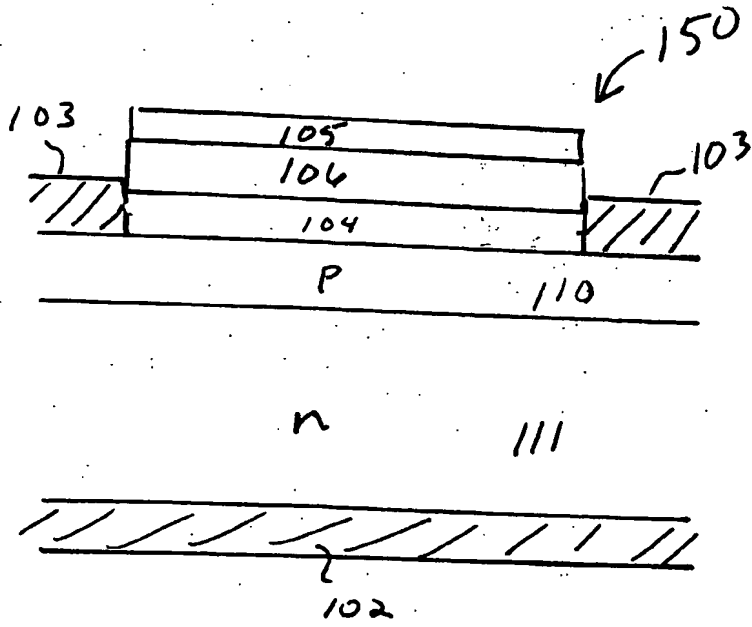


FIG. 4b

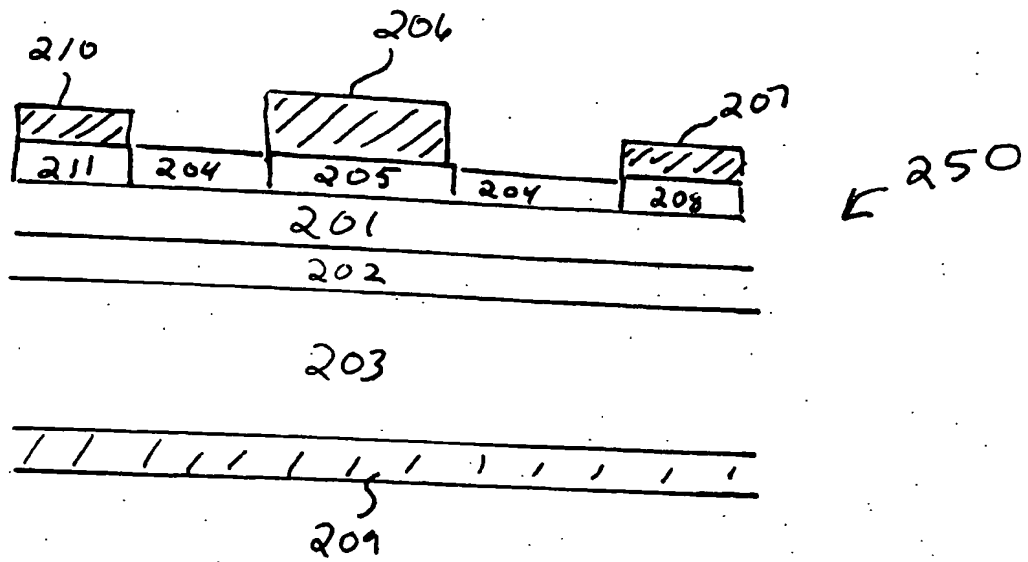


FIG. 5a

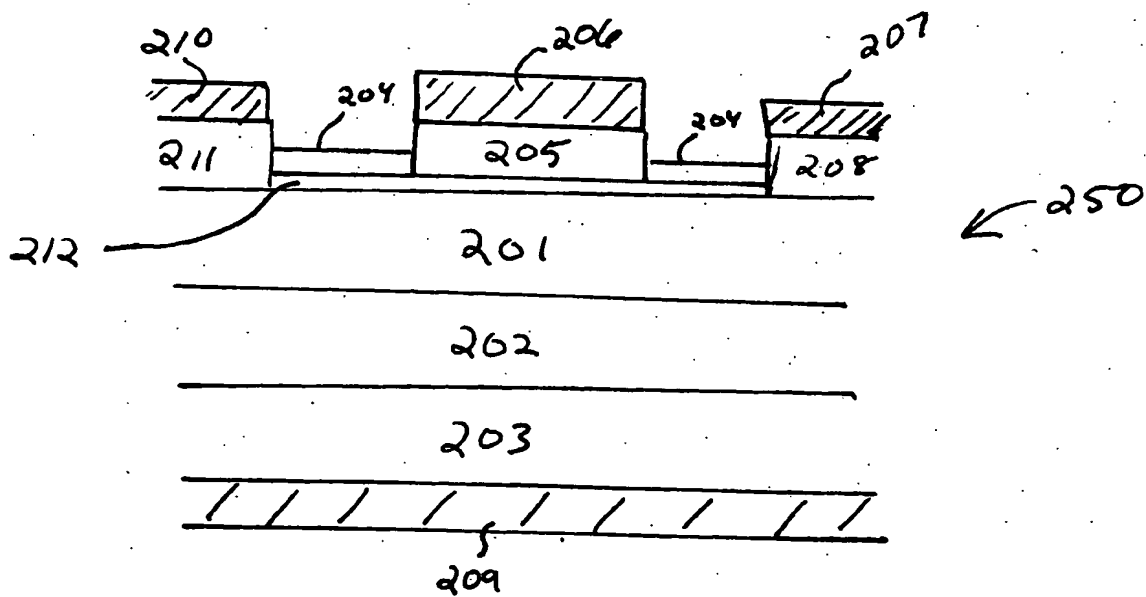


FIG. 5b

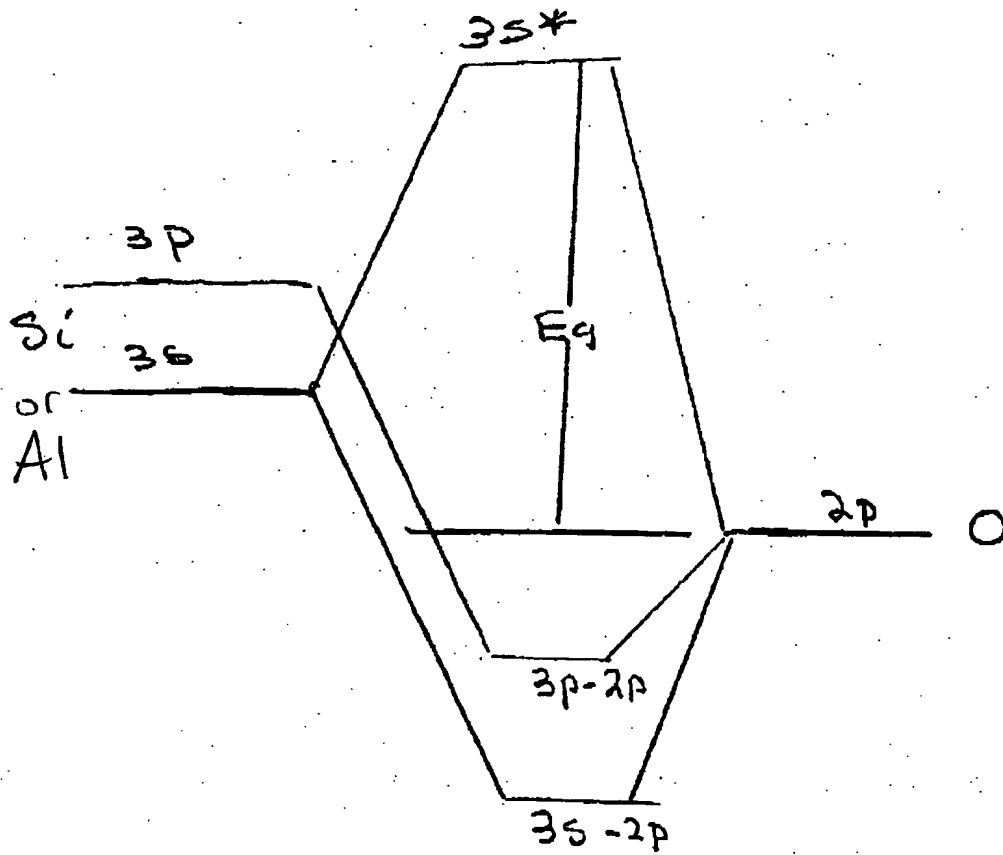


FIG. 6a

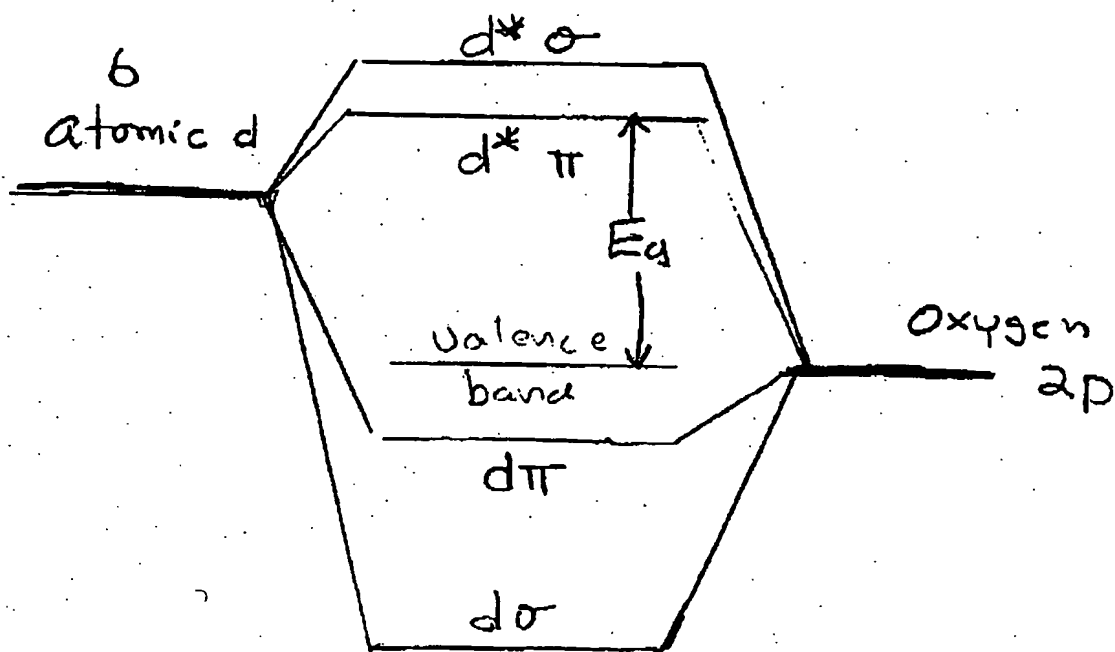
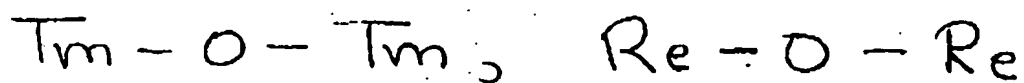


FIG. 6b

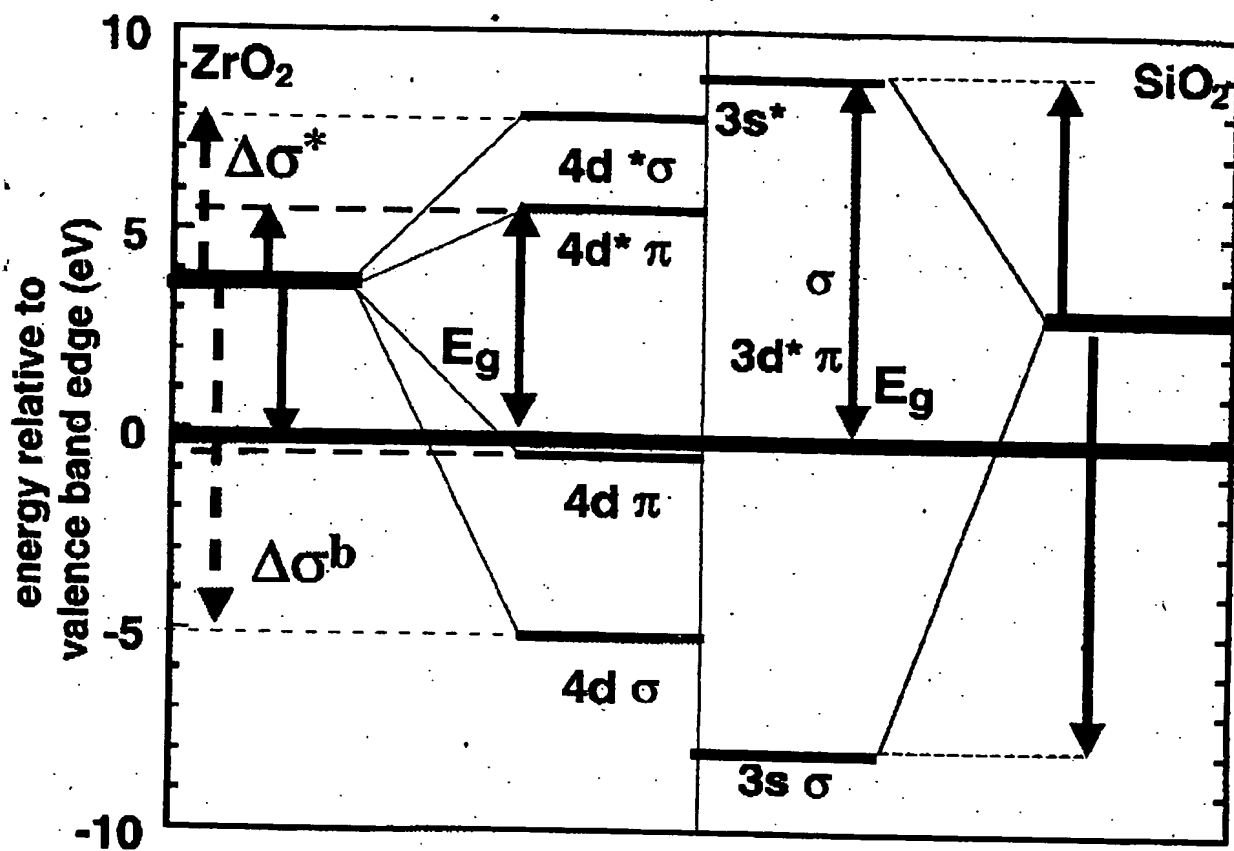


FIG. 6c



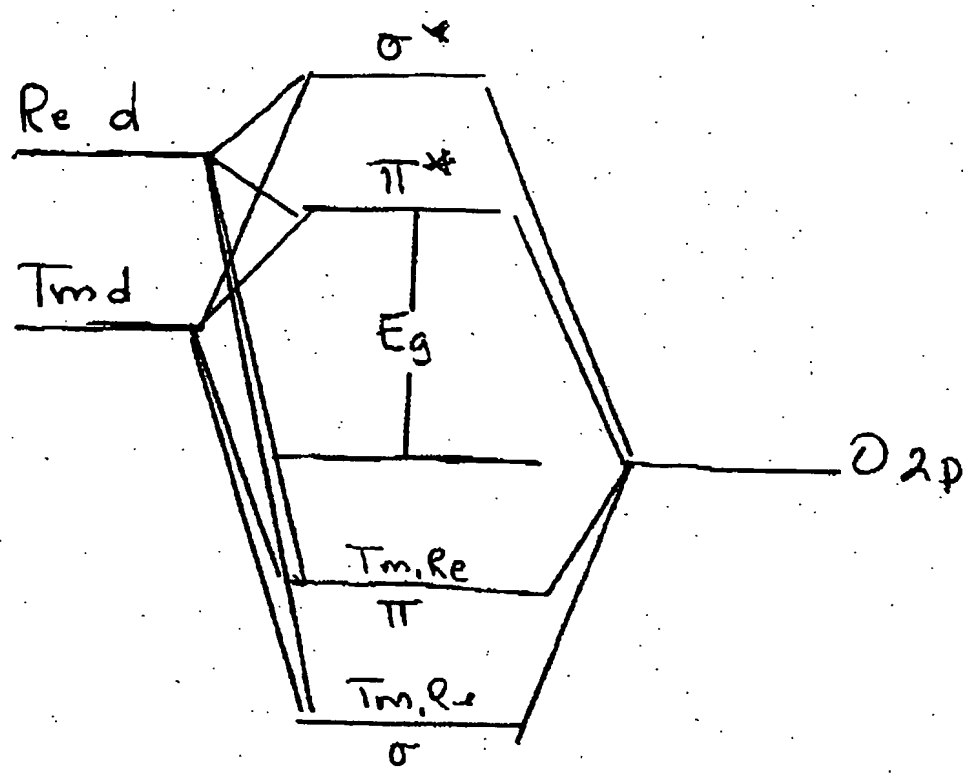


FIG. 6d

FIG. 7

